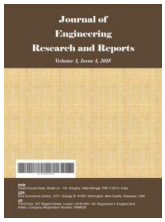

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Challenges and Resolution for Copper Wirebonding on Tapeless Leadframe Chip-on-Lead Technology

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Authors' contributions

This work was carried out in collaboration amongst the authors. Both authors read, reviewed, and approved the final manuscript.

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ABSTRACT

This technical paper discusses a methodological and systematic way of resolving key challenges during introduction of Chip-On-Lead package specifically wirebonding issues that leads to production dilemma during production ramp-up of products using copper wire in tapeless leadframe. The project was intended to determine the "Red-X" or the major cause of yield detractors that may lead to quality issue during wirebonding process.

Problem solving tools were showcased in this paper such as Data Analysis, Cause and Effect, Design-of–Experiment (DOE) and mechanical dimensional analysis which provided substantial impact in determining the real root-cause of the problem. Step-by-step elimination of variables was achieved with the use of statistical engineering tools. Outcome of the project eliminated the occurrence of Non-Stick-On-Pad (NSOP) during wirebonding process without cost involved and just optimizing the available in-house resources. The improvements also enhanced the quality of the product after final test which on the other hand lower the risk of having potential customer complaint in the future.

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Keywords: Chip-on-lead; tapeless leadframe; copper wirebonding; non-stick-on-pad; wirebond; design-of-experiment.

1. INTRODUCTION

In order to cope and adapt to the fast-paced changing technology in Semiconductor Industry, one should be flexible and resourceful in embracing the change, to have a very good impression from the customer. This is one of the biggest challenges for any semiconductor company in order to maintain its competitive market position and value. Conversely, failure to provide customer expectation will result to possible business failure.

The development of Copper (Cu) wire is the biggest leap today on the semiconductor industry providing cost efficient and high power devices [1-3]. Copper wire provides better conductivity than Gold (Au) and Aluminum (Al), in which helps offer a better heat dissipation and increased power ratings even with thinner wire application. Another outstanding characteristics of Copper compared to Gold is its mechanical properties, it demonstrate excellent ball to neck strength and high loop stability during encapsulation process. The integration of Copper wire technology has been a big challenge in semiconductor manufacturing. This new technology has provided manufacturability apprehensions at wirebond process, specifically on the latest portfolio of Chip-On-Lead (COL) tapeless leadframe-based packages. With the introduction of Copper wire, COL package, and the tapeless leadframe, wirebonding process becomes complicated and more challenging. With the continuing technology trends and state-of-the-art platforms [4-6], this technical paper discusses how the challenges were turned into milestones when top yield detractors of critical processes were addressed by in-depth engineering analysis and utilizing statistical tools at early stage of production.

1.1 Chip-on-Lead Package Construction

Chip-On-Lead (COL) is a technology where die or crystal is mounted on the leads of the leadframe instead of the paddle. To make it complicated, this leadframe has no tape for support during wirebonding unlike conventional leadframe. COL packages have not only provided a low cost solution on reducing body size requirements, but also have shown proven package robustness meeting target reliability performances and key quality and productivity indices that enabled a production worthy package. Shown in Fig. 1 and Fig. 2 are the package cross-section view and the typical molded package outline of COL package, respectively.

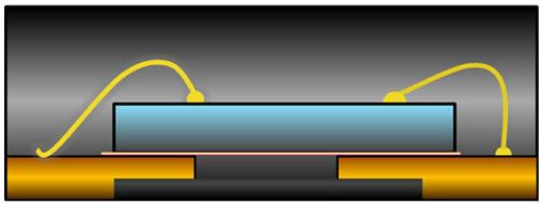


Fig. 1. Chip-on-Lead (COL) package cross-section view

Fig. 2. Typical molded COL package outline

1.2 Copper Wire in Thermosonic Wirebonding

Wirebonding is the process of providing electrical connection between the silicon chip and the external leads of the semiconductor device using very fine bonding wires. The wire used in wirebonding is usually made either of Gold (Au) or Aluminum (Al), although Copper (Cu) wires are starting to gain attention in the semiconductor manufacturing industry. There are two common wirebond processes: ball bonding and wedge bonding.

In the case of the package or device in focus (hereinafter referred to as Device C), Copper wire and ball bonding is being used. Fig. 3 illustrates the overview of the wirebond process. During ball bonding, a ball is first formed by melting the end of the wire (which is held by a bonding tool known as a capillary) through Electronic Flame-Off (EFO). This free-air ball has a diameter ranging from 1.5 to 2.5 times the wire diameter. Free air ball size consistency, controlled by the EFO and the tail length, is critical in good bonding. The free-air ball is then brought into contact with the bond pad. Adequate amounts of pressure, heat, and ultrasonic forces are then applied to the ball for a specific amount of time, forming the initial metallurgical weld

between the ball and the bond pad as well as deforming the ball bond itself into its final shape. The wire is then run to the corresponding finger of the leadframe, forming a gradual arc or "loop" between the bond pad and the lead finger. Pressure and ultrasonic forces are applied to the wire to form the second bond (known as a wedge bond, stitch bond, or fishtail bond) this time with the lead finger. The wire bonding machine or wire bonder breaks the wire in preparation for the next wire bond cycle by clamping the wire and raising the capillary.

1.3 The Chip-on-Lead Tapeless Leadframe

Tapeless Chip-On-Lead package is a leadframe-based package carrier or platform in which the leads footprint will be formed by back-etching process. The plant has a lot to gain with tapeless package – cheaper leadframe cost, Copper wire compatible, no tape and faster sawing speed in singulation. Shown in Fig. 4 is the tapeless leadframe configuration.

1.4 Cost Impact of Copper Wire and Its Performance

The device technology trend continues to become critical and complex. The plant launched the very first product that uses Copper in wirebonding and tapeless leadframe for COL package. Knowing the price of Copper wire is 75% cheaper than its Gold counterpart, once materialized it will bring a lot of savings and will create more business in the plant. But like any other new products, this product faced a lot of challenges that later on transformed into milestones.

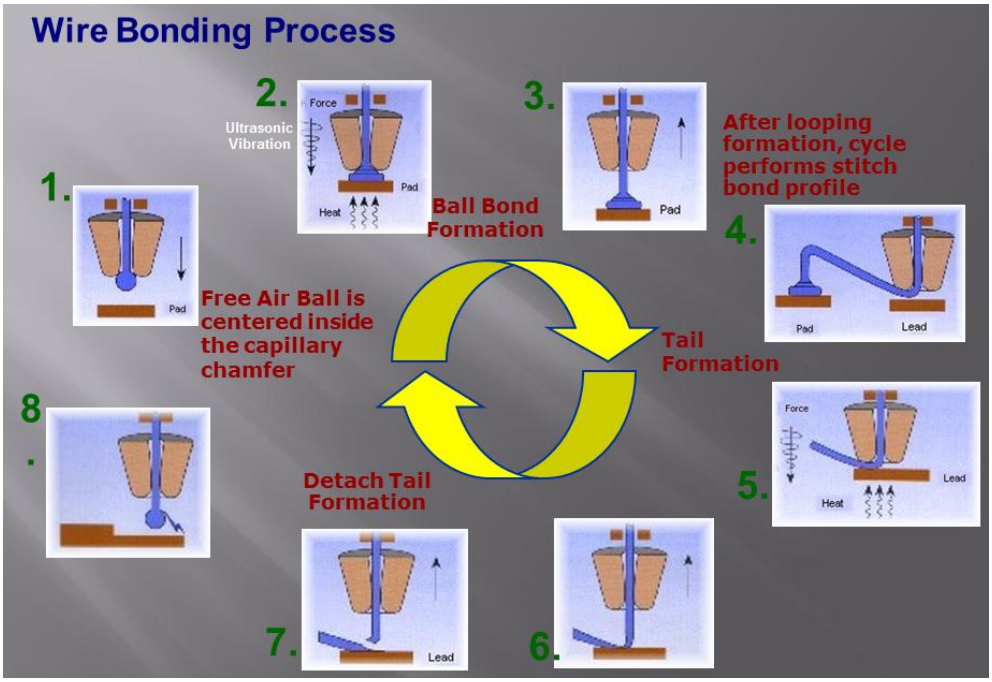


Fig. 3. Wirebonding process mechanism

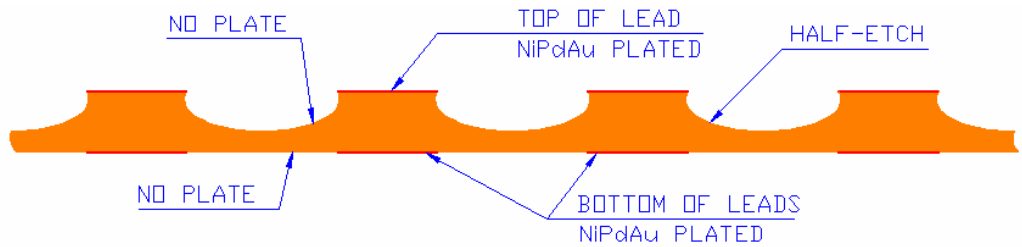


Fig. 4. Tapeless leadframe configuration

Aside from being cost efficient, Copper has several advantages over Gold. First, Copper has a lower resistivity (resistivity = 17.24 Ω-m) compared to Gold (resistivity = 23.26 Ω-m) which allows more signals to flow at a given time. Copper helps improve increased device power ratings even with thinner wire application. Furthermore, the electrical conductivity (reciprocal of resistivity) is a major advantage of Copper over Gold; in fact it is 25% better. Electrical conductivity of Copper is $5.8x10^7$ Siemens/m while Gold is at $4.3x10^7$ Siemens/m. In line with this Copper wire can be used for higher performance of fine pitch applications (smaller pad sizes), power management devices and increases operating current of the device. The third major advantage of Copper wire is its thermal conductance. Copper has 39.5 kW/m² K compared to Gold of 31.1 kW/m² K. Some of the benefits of this characteristic is better heat dissipation in package, low risk of recrystallization when heat is applied and low loop applications. Lastly, one of the major differences of Copper versus Gold is in its intermetallic growth Gold intermetallic growth significantly increased over time, which makes the bonding interface brittle. On the other hand, Copper have lower Inter-Metallic Coverage (IMC) growth which increases bonding strength. Slower IMC growth also helps improved device reliability and performance because of lower electrical resistance and lower heat generation.

1.5 Device in Focus

Device C is an Electrically Erasable Programmable Read-Only Memory (EEPROM) device with CMOSF8HP4 die technology and packaged in a tapeless leadframe configuration. The package thickness is at 0.55 mm, with only 5 leads or pins or pads. Shown in Fig. 5 is the device configuration.

1.6 Full Process Flow

During initial phase of the investigation, all possible variables to determine the yield loss contributors were studied. In the case of Device C, the entire processes were analyzed as this product carries new process bricks and technology for the plant such as Copper wirebonding and the use of tapeless leadframe which is more sensitive than the conventional leadframe. An overview of the assembly process flow is illustrated in Fig. 6. It is worth noting that process flow varies with the product and the technology [7-9].

Fig. 5. Device C configuration

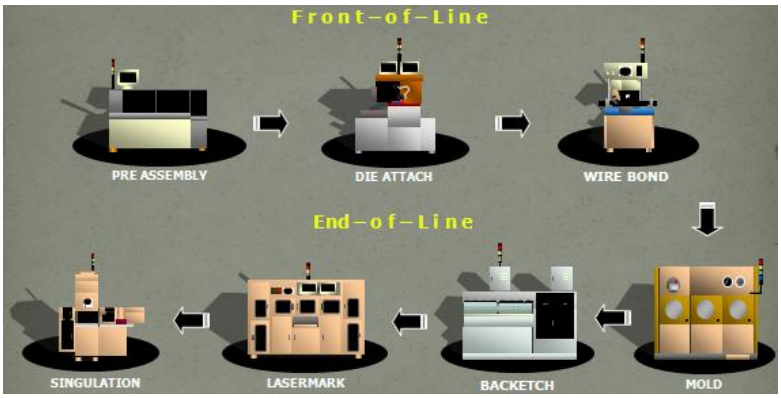


Fig. 6. Device C assembly process flow

During the investigation, it was established that the major source of yield loss during ramp-up stage is wirebond. This is a substantial finding so that attention and effort for the root-cause analysis will only focus on this process. Furthermore, yield detractors and top defects were also identified by collecting defect signatures that will serve as lead to further investigate and analyze the root-cause of the problems. Pareto diagram in Fig. 7 shows the yield loss contribution per process and their corresponding rejection rate as source of yield loss during ramp-up stage.

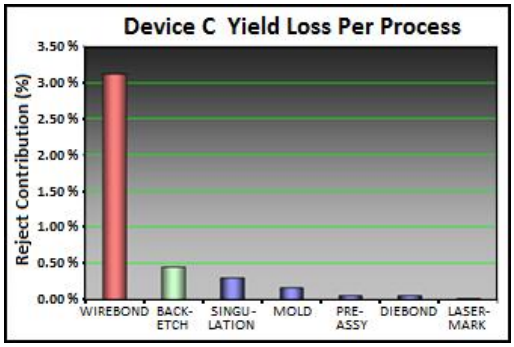


Fig. 7. Pareto diagram of yield loss contributor per process

Wirebond has ~3.0% yield loss and considered as high priority among other assembly processes. Furthermore, Problem Definition Tree was established, a structured step-by-step statistical tool used in the analysis to systematically guide the team and identify the top priority. Shown in Fig. 8 is the Project Definition Tree (PDT) where all factors affecting the Device C low yield were considered and comprehended.

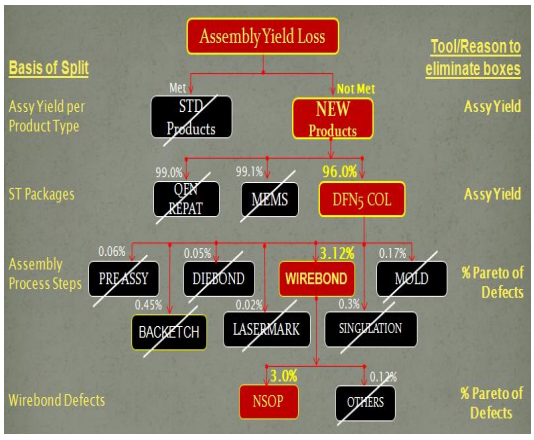


Fig. 8. Problem definition tree

In order to have a lead on the problems for each process, actual defects were collected, studied and analyze deeper based on defect signatures. Shown in Fig. 9 is the defect signature of Non-Stick-On-Pad (NSOP) during wirebond process.

Several lots during ramp-up in production were severely affected and way above the allowable Parts Per Million (PPM) level of 0.5%, as shown in Fig. 10.

1.7 Problem Statement

NSOP with an average of 3.0% rejection rate per lot is classified as wirebonding related defects provide significant failure that substantially affects the assembly yield with only ~96% during ramp-up stage of Device C.

Majority of the process batches were put on-hold and visually inspected due to alarming high rejection rate not meeting the 0.5% NSOP baseline criteria. Batches having NSOP > 0.5% were evident per lot during ramp-up.

2. EXPERIMENTAL SECTION

2.1 Root-Cause Analysis: Fishbone Analysis

To capture all variables or potential causes leading to NSOP, Fishbone Diagram in Fig. 11 and Cause and Effect Diagram were employed. Each of the causes was validated to come up to the true causes. Shown in Table 1 is the validations made.

2.2 Focusing on NSOP (Non-Stick-on-Pad)

For wirebond, based on Pareto Principle, the top defect contributor is NSOP (3.0%). The 0.12% other defects (trivial many – composed of many small percentage of defects) was not included in the analysis to save time and effort. Shown in Fig. 12 is the NSOP occurrence in 5 pads of Device C.

Sample photos of bonded units showing NSOP manifestation on pads 1 and 2 are shown in Fig. 13. Similar manifestation occurred on pads 3, 4, and 5.

Machine-to-machine validation was also performed to check if NSOP defect is not machine related. The comparison is shown in Fig. 14.

Fig. 9. NSOP wirebond defect characterization

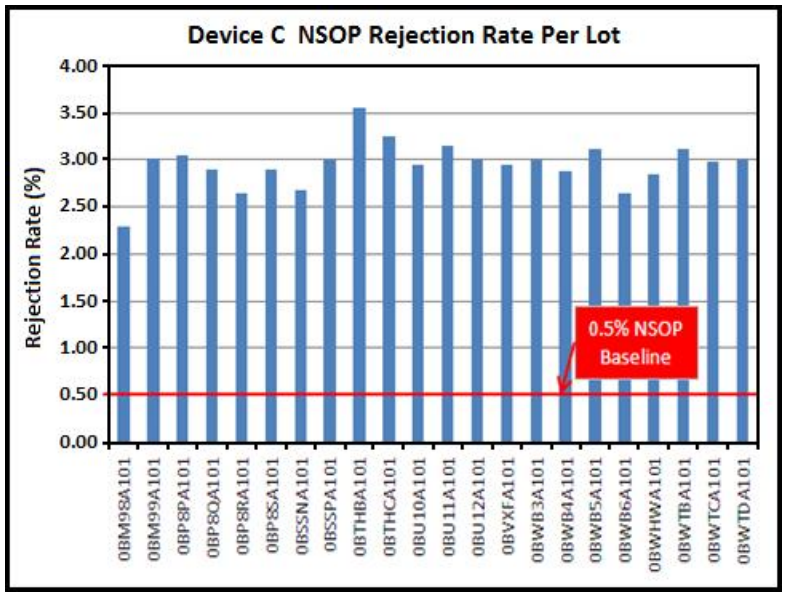


Fig. 10. NSOP rejection rate per lot

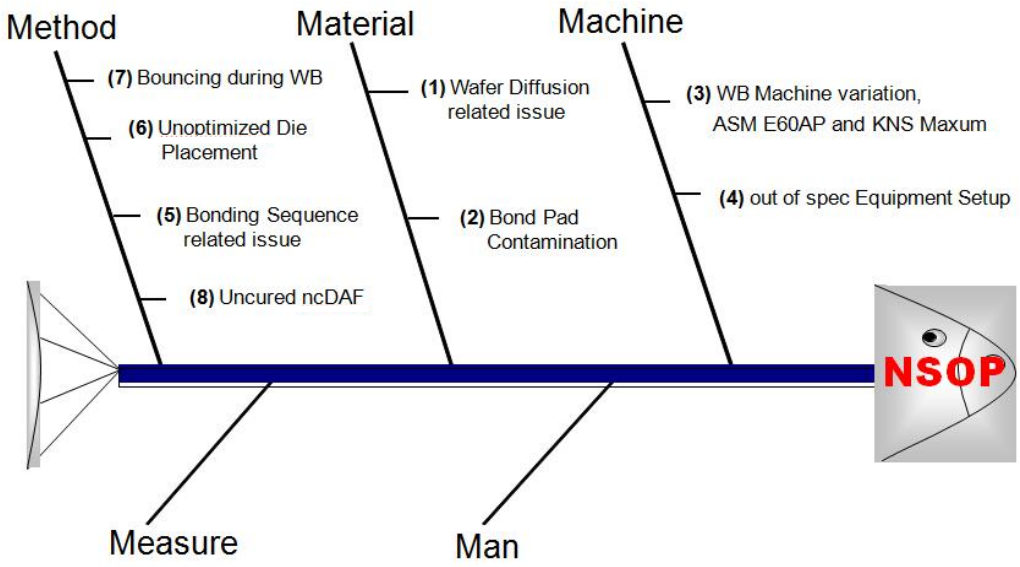


Fig. 11. Fishbone diagram

Table 1. Potential cause validation

Potential cause		Method of validation	Result of validation	Conclusion
1	Wafer diffusion	Check if problem is isolated on a particular diffusion	All diffusions are affected by NSOP	Not True Cause
2	Bond pad contamination	Perform Energy-Dispersive X-ray Spectroscopy (EDX) analysis on affected pads	No contamination detected	Not True Cause
3	Wirebond machine variation	Check machine1 and machine2 for NSOP response	Both machines manifest NSOP occurrences	Not True Cause
4	Out of specification equipment setup	Check equipment parameters for TVC, Air Flow, Vacuum, and Temp	Pertinent parameters within specification	Not True Cause
5	Bonding sequence related issue	Compare NSOP occurrence when reverse bonding sequence is used	NSOP is encountered at 7/30 units	Not True Cause
6	Un-optimized die placement	Optimize die placement through Design-of-Experiment (DOE)	NSOP is encountered at 6/30 units	Not True Cause
7	Bouncing during wirebonding	Use high-speed camera to check manifestation of bouncing at pad area during wirebond	Bouncing phenomenon observed: 8/30 NSOP is due to clamp and inserts	True Cause
8	Uncured non-conductive Die-Attach Film (ncDAF)	Check the Differential Scanning Calorimetry (DSC) of material	ncDAF is fully cured	Not True Cause

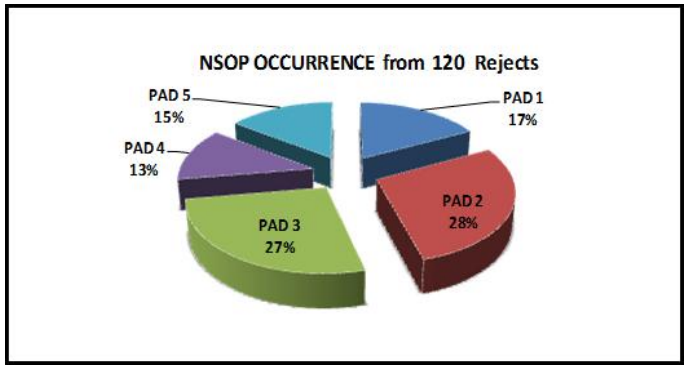


Fig. 12. NSOP pie chart

Table 1, which was earlier presented, shows the validation made on all wirebond machined being used to process Device C. Significant differences in ball shear results were observed, as illustrated in Fig. 15 using SAS-JMP software [10], a statistical tool that calculates automatically the combination of runs. Readings from pads 2 and 3 are passing but are significantly lower than those of pads 1, 4, and 5.

The same diffusion wafer batch was split into three wirebonding machines but gave the same results and level of NSOP rejects. With that, wirebond machine was set aside in the investigation.

2.3 Why-Why Analysis

Digging deeper, further validation was made through Why-Why Analysis as exemplified in Table 2. This confirms that the “Red-X” is the configuration of the designed insert used during the line stressing lot of Device C, causing the NSOP rejection.

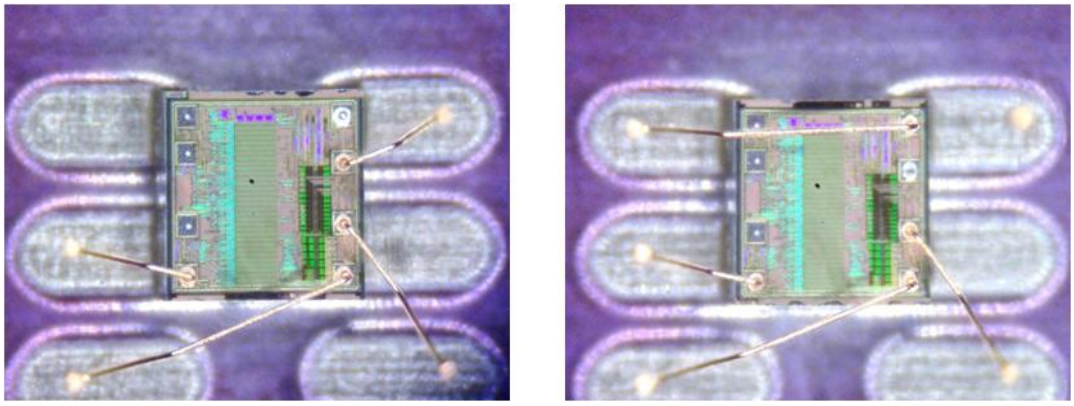


Fig. 13. NSOP defect mechanism

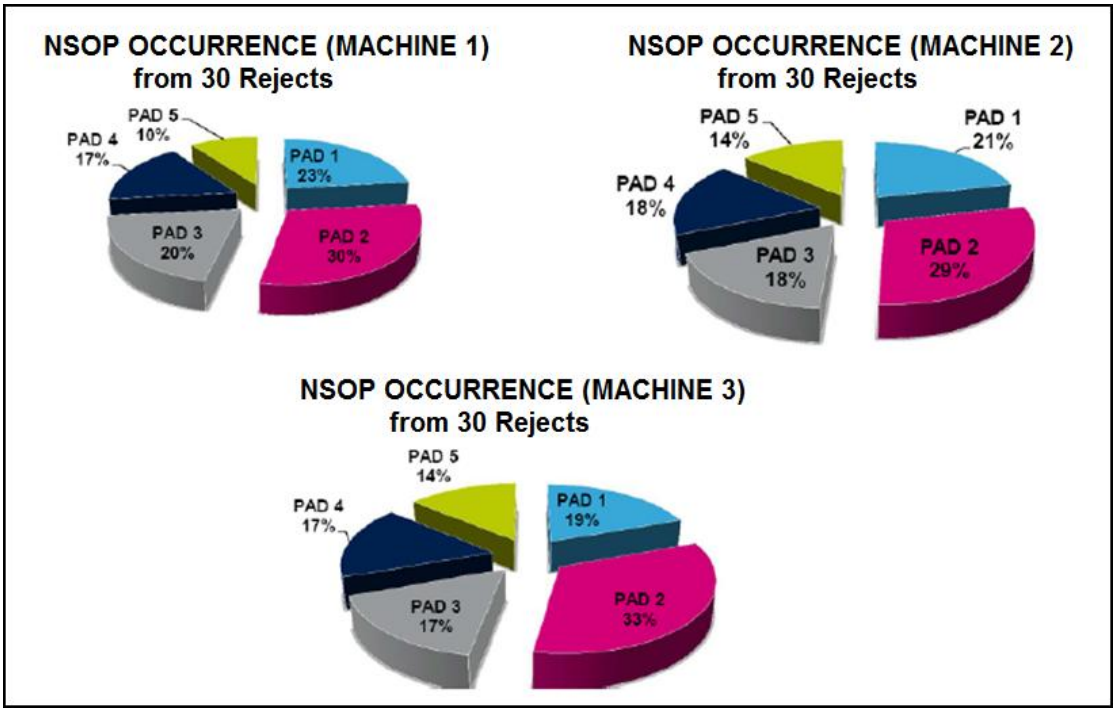


Fig. 14. Wirebond machine-to-machine comparison

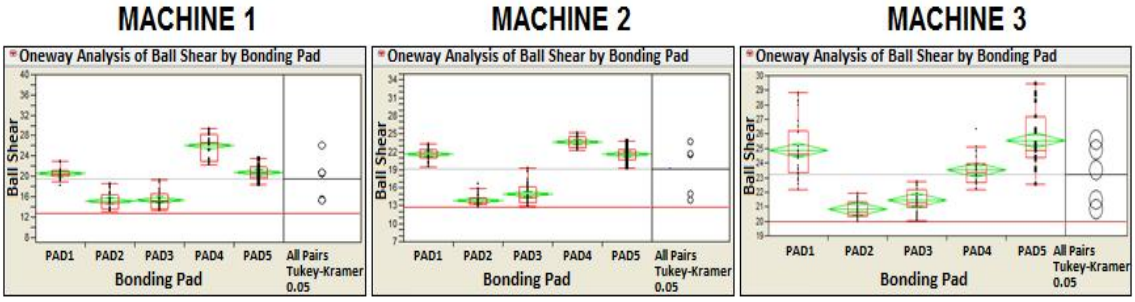


Fig. 15. Wirebond machines statistical analysis

More holes on the insert avoid air traps in between units and eventually flatten the leadframe during vacuum at wirebonding. Fig. 16 compares the old insert design and the new insert design.

A flattened leadframe results to better wirebond quality and less probability of NSOP occurrence. Table 3 and 4 present the Why-Why Analysis of systematic root-cause and escape root-cause, respectively.

Table 2. Technical root-cause why-why analysis

Why 1	Why 2	Why 3	Why 4	Why 5	Why 6
Bouncing on leadframe pad area during wirebond resulting to NSOP	Leadframe pad area is not firmly hold upon vacuum activation after panel clamping	Presence of entrapped air between leadframe and insert	Air is not able to escape through the designed holes in the insert	Vacuum holes are located too far apart (not fit for Device C density)	It is the configuration of the designed insert used for the affected 2nd line stressing lot of Device C

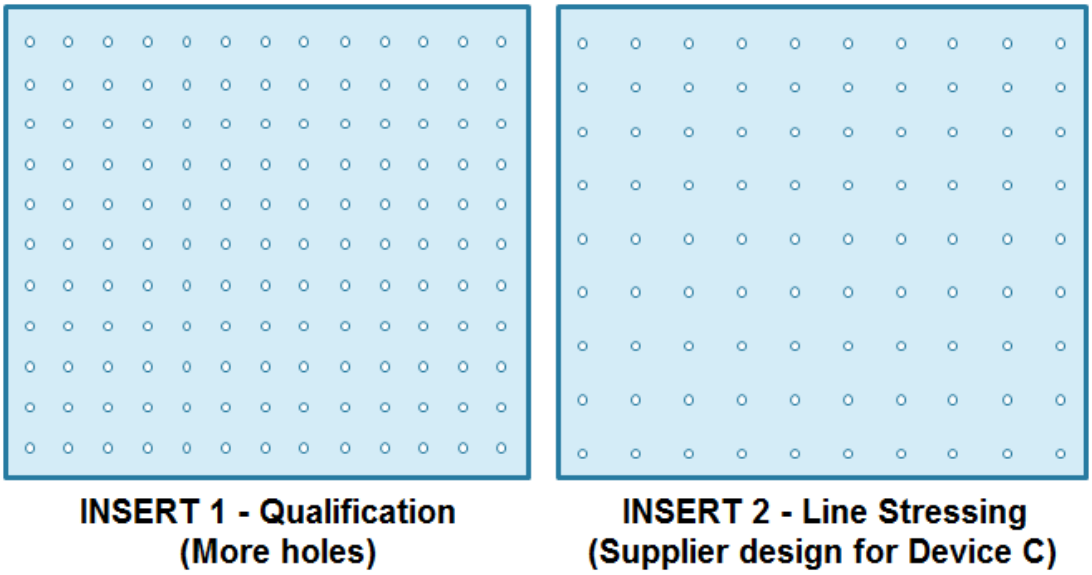


Fig. 16. Old and new inserts comparison

Table 3. Systematic root-cause why-why analysis

Why 1	Why 2	Why 3	Why 4	Why 5
It is the configuration of the new insert used for the affected 2nd line stressing lot of Device C	The configuration of the insert was designed by the supplier based on the LF drawing provided (in reference to the requested design change for the window clamp The change in insert configuration (from qualification to line stressing) was not detected upon delivery and use Focus is on the requested change in clam window opening	As per current practice for clamp and insert design for new products No incoming buy-off or inspection done for the new clamp and insert	Buy-off of clamp and insert not part of the procedure Only functional buy-off is done (on actual unit processing)	

Table 4. Escape root-cause why-why analysis

Why 1	Why 2	Why 3	Why 4	Why 5
Not Applicable				
NSOP was effectively detected by the current control (alarm) during wirebond				

3. RESULTS AND DISCUSSION

Results of comprehensive investigation through Fishbone and Why-Why Analysis showed that the root-cause of HIGH NSOP Rejection rate can be attributed to clamp and insert design, most particularly the insert design. This was identified after series of analysis and validation using different runs. The results was further strengthened by using a high speed camera that helped pinpoint the root-cause of the NSOP phenomena. Results revealed that by using the modified insert design with more holes will address NSOP rejection without sacrificing quality requirements of the products including reliability.

3.1 New Clamp and Insert Design

A Design-of-Experiment (DOE) for 1st bond parameters was conducted with the objective to determine and define window that will minimize occurrence of NSOP. New insert design (Rev 1) shown in Fig. 17 has total of 1,415 holes to hold 680 units per panel while the original insert design (Rev 0) has only 220 holes.

T-Test or Analysis of Variance in Fig. 18 revealed significant difference using new design or parameter over the previous design.

3.2 On-Off Validations

To strengthen the premise on NSOP is due to clamp and insert design. Wirebond parameters were brought back to its original set-up. Employing On-Off validation, it is evident in Fig. 19 that new clamp and insert dictates the outcome of NSOP rejection rate. Results of all experiments and validation runs strengthen the conclusion that the NSOP due to poor design of clamp and insert can be mitigated using higher new design with enhanced vacuum capability.

3.3 Response on Critical Product Characteristics

To further verify if the new set of parameters will satisfy the quality requirements based on the plant's standards, critical responses were studied and collected. Evaluation results are shown in Fig. 20 to 23.

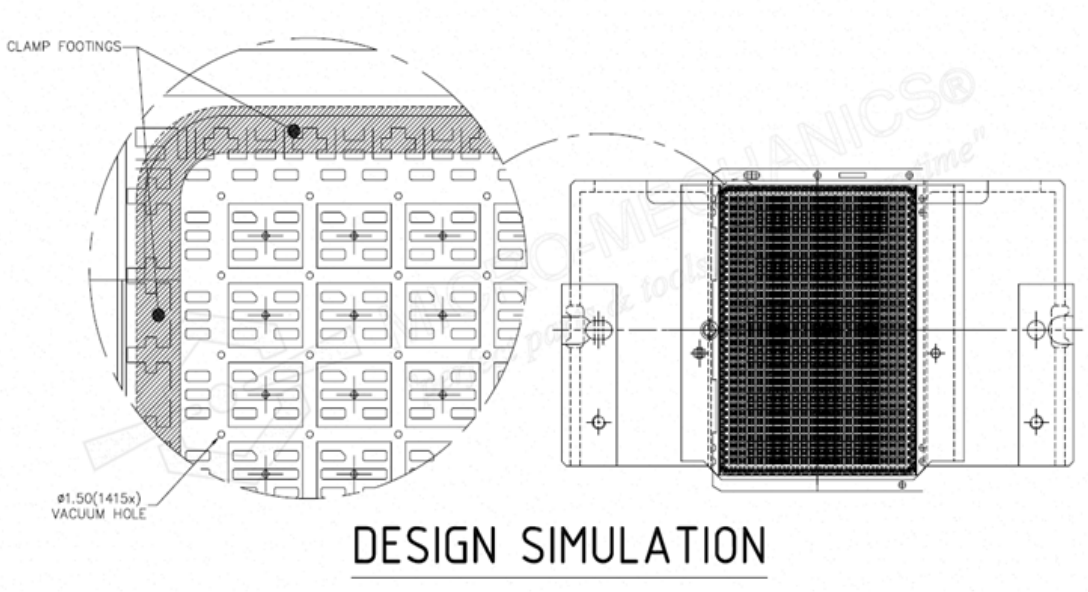


Fig. 17. New design of clamp and inserts

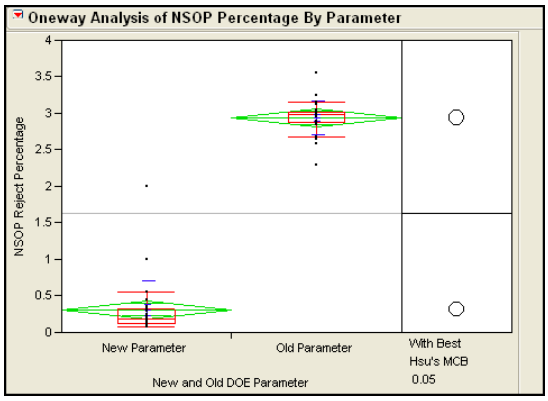


Fig. 18. Statistical analysis graph showing significant difference between parameters on old and new clamp and insert design in terms of NSOP attribute data

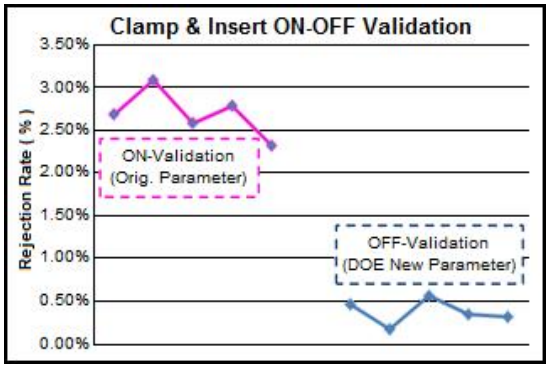


Fig. 19. Clamp and insert design/parameters On-Off validation

Parameter	Ball Shear	Wirepull	Remarks
LOW SIDE (LL)			PASSED Quality Requirements
NOMINAL (MID)			PASSED Quality Requirements
HIGH SIDE (HH)			PASSED Quality Requirements

Fig. 20. Ball shear and wire pull test results

3.4 Solution Implementation and Mass Production

After replacement of new clamp and insert design that mitigates the risk of NSOP defects and validations in terms of Quality and Reliability aspects, large scale evaluations were made through Line Stressing to validate effectiveness of new clamp and insert design. Error proofing was employed to identify actions that will either control or eliminate these errors.

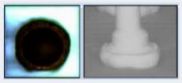
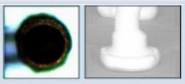
Parameter	Ball Profile	Remarks
LOW SIDE (LL)		PASSED Quality Requirements
NOMINAL (MID)		PASSED Quality Requirements
HIGH SIDE (HH)		PASSED Quality Requirements

Fig. 21. Ball profile results

Parameter	Cratering	Remarks
LOW SIDE (LL)		PASSED Quality Requirements :NO bond pad damage observed
NOMINAL (MID)		PASSED Quality Requirements :NO bond pad damage observed
HIGH SIDE (HH)		PASSED Quality Requirements :NO bond pad damage observed

Fig. 22. Cratering results

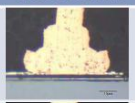
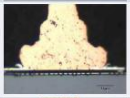
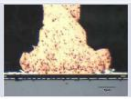
Parameter	Cross Section	Remarks
LOW SIDE (LL)		PASSED Quality Requirements : Fully ball bond flatness
NOMINAL (MID)		PASSED Quality Requirements : Fully ball bond flatness
HIGH SIDE (HH)		PASSED Quality Requirements : Fully ball bond flatness

Fig. 23. Cross-section results

Continuous monitoring on the lots during mass production was carried out. Result of verification, showed that the lot using new clamp and insert design has an average of 0.32% reject rate. NSOP trend together with the action and date of execution was monitored to confirm and validate the effectiveness of the implemented solution. Shown in Fig. 24 is the detailed monitoring graph regarding NSOP before and after the solution implementation.

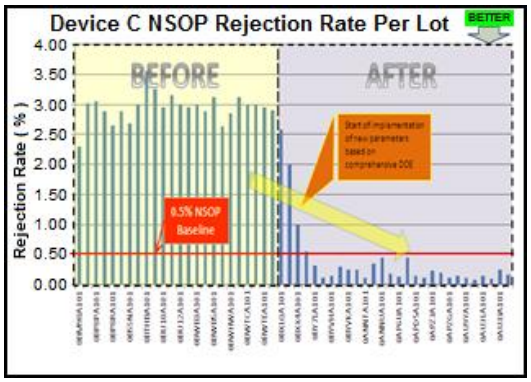


Fig. 24. NSOP lot trend before and after the implementation of the corrective actions

Other factors were also measured particularly scrapping of lots due to high NSOP rejection. Fig. 25 illustrates the positive impact after the implementation of corrective action.

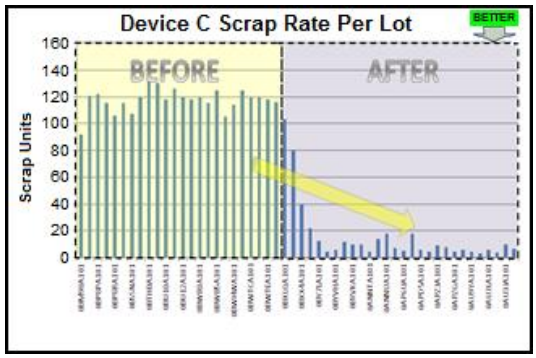


Fig. 25. Scrap rate improved after implementation of corrective actions

Significant effect was felt in the Scrap rate. Moreover, assembly yield shown in Fig. 26 increased by more than 3% and meeting the wirebond yield of 99.5%. Yield trend stabilized after the implementation of corrective action.

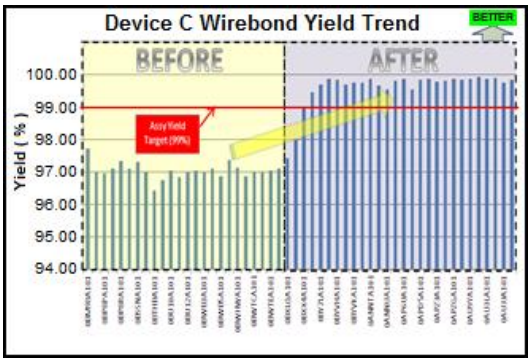


Fig. 26. Assembly wirebond yield trend

4. CONCLUSION AND RECOMMENDATIONS

In-depth methodological analysis and statistical techniques for solving the NSOP defects were presented on this paper. Using the knowledge and understanding on data and defect phenomena lead us to pinpoint the true cause of this defect. Comprehensive Why-Why Analysis and Validation mitigates the NSOP rejects which are attributed to design of insert used during qualification affecting the performance Cu wirebonding of Device C package. By changing the design of the clamp and insert occurrence of NSOP rejects as manifested during line stressing and validation of run. NSOP defect was solved without too much cost involved and no major modification on the assembly process.

It is recommended that the corrective actions be identified and be fanned out to other on-going package development. Relevant procedure should be updated to include the clamp and insert design review with suppliers and internal stakeholders. Corresponding buyoff procedure should also be updated.

It is also recommended that the assembly and test manufacturing processes observe proper Electrostatic Discharge (ESD) controls. Opportunities presented in [11,12] could be very useful to help ensure ESD check and controls. Ultimately, continuous improvement is important for sustaining the quality excellence of any product and of the assembly and test plant.

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COMPETING INTERESTS

Authors have declared that no competing interests exist.

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