Journal of Engineering Research and Reports

14(3): 30-33, 2020; Article no.JERR.58934
ISSN: 2582-2926

ESD Diode Protection Incorporated on Leadframe Package

Frederick Ray I. Gomez[1*], Edwin M. Graycochea Jr.[1], Nerie R. Gomez[1] and Rennier S. Rodriguez[1]

[1]STMicroelectronics, Inc., Calamba City, Laguna, 4027, Philippines.

Authors' contributions

This work was carried out in collaboration amongst the authors. All authors read, reviewed and approved the final manuscript.

Article Information

DOI: 10.9734/JERR/2020/v14i317126
Editor(s):
(1) Dr. Heba Abdallah Mohamed Abdallah, National Research Centre, Egypt.
Reviewers:
(1) I. Dhanya, Mahatma Gandhi University, India.
(2) Tsafack Nestor, University of Dschang, Cameroon.
Complete Peer review History: http://www.sdiarticle4.com/review-history/58934

Short Research Article

Received 27 April 2020
Accepted 03 July 2020
Published 16 July 2020

ABSTRACT

With the new die technology becomes smaller and thinner, silicon die circuit metallization also becomes smaller, thus electronic devices like quad-flat no-leads multi-row (QFN-mr) semiconductor leadframe package design become more sensitive and prone to electrostatic discharge (ESD) damages. This paper focused and introduced an additional surface mount technology by attaching diodes before and after diebonding process to protect the whole package and to prevent package related issues encountered. With this diode attached on the silicon die and leads, added protection could be achieved on the integrated circuit (IC) mounted on the circuit board level.

Keywords: QFN-mr; ESD; leadframe; diode attach.

1. INTRODUCTION

New technologies in semiconductor assembly manufacturing are very sensitive in terms of electrostatic discharge (ESD) that can affect the whole integrated circuit (IC) mounted on the board level. With time-to-market customer needs becoming more demanding, there is a necessity to adapt to the latest trends, prevent package-related issues, and address issues at the soonest as possible. The development of quad-flat no-leads (QFN) and QFN multi-row (QFN-mr)

**Corresponding author: Email: f.i.gomez@ieee.org, frederick-ray.gomez@st.com;*

device has changed from the standard assembly flow to an advanced process with ESD diode attachment. This paper aimed to eliminate the package issue encountered on the board level that is caused by ESD, with damage resulting to burnt parts for example as shown in Fig. 1. Discussion on the fundamentals of ESD and ESD damage could be found in the ESD Association references and previous works [1-2].

2. METHOD OF ASSEMBLY AND PROBLEM STATEMENT

The standard QFN assembly process flow is shown in Fig. 2. which includes pre-assembly, die attach, wirebond, mold and singulation. Note that QFN and QFN-mr process flow differs on the advanced process flow described in Fig. 3. Moreover, it is important to note that assembly process flow in general varies with the product and the technology [3-5]. Also, with new and continuous technology trends and state-of-the-art platforms, challenges are inevitable [6-8].

Pre-assembly process wherein the wafer is prepared and cut the silicon dies into pieces. Die attach is the process of attaching a semiconductor die either on a leadframe or in the substrate carrier. The method of attaching the silicon die to a leadframe or a carrier is formed using this type of technique: 1) The ejector needle pushing up from the wafer tape while the rubbertip serves as the collet to pick the silicon die. 2) Picked silicon die is placed on the leadframe or carrier. The difference between the standard die attach process and the advanced process as is the ESD diode attachment. ESD diode method of attachment is the same with die attach process and there is a temperature underneath the carrier so that the diode will stick. Attaching of ESD diode was introduced to achieve the required ESD protection on the board level to prevent shorting issues and ESD-related damages. And with this type new technology is very challenging to us to eliminate the current issue in semiconductor assembly manufacturing are inevitable.

3. PACKAGE DESIGN SOLUTION

The electronic packages in semiconductor leadframe configuration are embedded with ESD protection component with the ESD diode on the leads and/or the silicon die, as illustrated in Fig. 4. A sample of ESD diode solutions with its

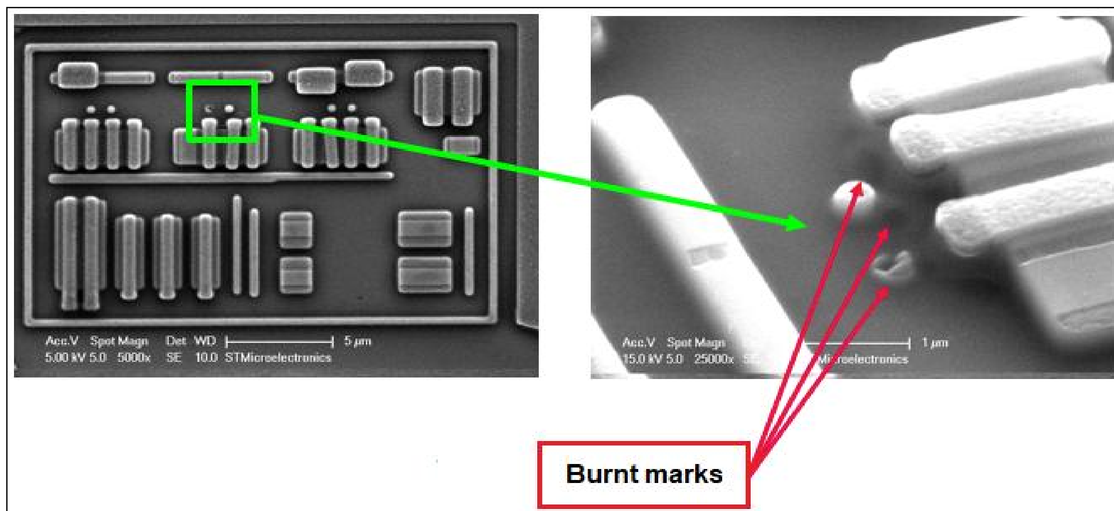

Fig. 1. ESD defect manifestation

Fig. 2. Standard QFN assembly process flow

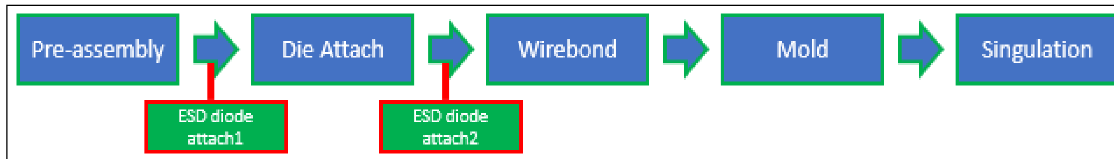

Fig. 3. Assembly process flow with diode attach process

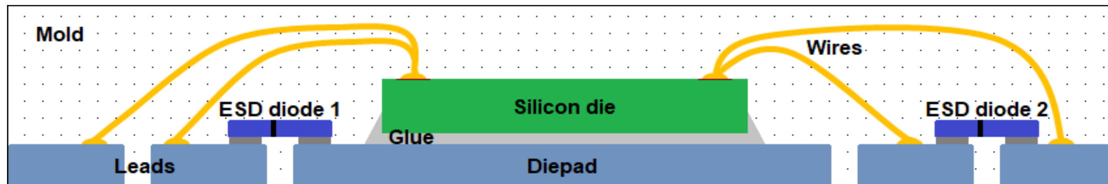

Fig. 4. QFN-mr package cross-sectional view

parameters could be accessed in the company's website [9]. In this paper, the ESD diode could be mounted or attached using conductive or sintered glue, solder bump, or any conductive adhesive material between the lead or signal pin and the diepad or ground, and could also be mounted between any two signal pins or leads depending on which signal pins are affected or need to be ESD-protected. By incorporating ESD protection components inside the electronic package, ESD-sensitive packages without internal ESD die circuitry could now be protected against eventual ESD-related defects or anomalies.

4. CONCLUSIONS AND RECOMMENDATIONS

The paper discussed the package solution by attaching of ESD diode to protect the whole package on the board level to prevent ESD-related damages. In this paper, an advanced assembly process is presented to realize the capability for ESD diode attach. Prototypes are helpful for future works to validate the effectiveness of the leadframe package. A comparison of this design solution should also be made with other works in the same field. Worth noting that the assembly manufacturing of leadframe packages should observe proper ESD checks and controls. Learnings shared in [2,10-11] are very helpful to realize proper and effective ESD-related controls.

ACKNOWLEDGEMENT

The authors would like to thank the New Product Development & Introduction (NPD-I) team and the Management Team (MT) for the continuous support.

COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. ESD Association. Fundamentals of ESD, device sensitivity and testing. USA; 2011.
2. Gomez FR, Mangaoang Jr. T. Elimination of ESD events and optimizing waterjet deflash process for reduction of leakage current failures on QFN-mr leadframe devices. Journal of Electrical Engineering, David Publishing Co. 2018;6(4):238-243.
3. May GS, Spanos CJ. Fundamentals of semiconductor manufacturing and process control. 1st ed., Wiley-IEEE Press, USA; 2006.
4. Nenni D, McLellan P. Fabless: The transformation of the semiconductor industry. Create Space Independent Publishing Platform, USA; 2014.
5. Harper C. Electronic packaging and interconnection handbook. 4th Ed., McGraw-Hill Education, USA; 2004.
6. Tsukada Y, Kobayashi K, Nishimura H. Trend of semiconductor packaging, high density and low cost. 4th International Symposium on Electronic Materials and Packaging, Taiwan; 2002.
7. Liu Y, Irving S, Luk T, Kinzer D. Trends of power electronic packaging and modeling. 10th Electronics Packaging Technology Conference, Singapore; 2008.

8. Sumagpang Jr. A, Rada A. A systematic approach in optimizing critical processes of high density and high complexity new scalable device in MAT29 risk production using state-of-the-art platforms. Presented at the 22nd ASEMEP Technical Symposium, Philippines; 2012.
9. STMicroelectronics. ESD protection. Available:https://www.st.com/en/protection-devices/esd-protection.html
10. Gomez FR. Improvement on leakage current performance of semiconductor IC packages by eliminating ESD events. Asian Journal of Engineering and Technology. 2018;6(5).
11. Gomez FR, Mangaoang Jr. T, Talledo J. Protection from ESD during the manufacturing process of semiconductor chips. US patent no. US10388594; 2019.

© 2020 Gomez et al.; This is an Open Access article distributed under the terms of the Creative Commons Attribution License (http://creativecommons.org/licenses/by/4.0), which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited

Peer-review history:
The peer review history for this paper can be accessed here:
http://www.sdiarticle4.com/review-history/58934